AMENDMENTS TO THE DRAWINGS:

The attached replacement sheet of drawings replaces the original sheet including Figs. 1, 2a, and 2b. No new matter is believed to have been entered.

REMARKS

Claims 1-20 are pending in this application, with claims 1, 8, and 16 being independent. Favorable reconsideration and reexamination of the action mailed on September 21, 2007 is respectfully requested in view of the following comments:

As required by the Office Action, Applicant has submitted replacement drawing sheets for Figures 1, 2a, and 2b, and Applicant has changed the title of the application.

Independent claim 1 recites a controller that includes a control circuit, an error signal generator, and a detector. The control circuit includes a forward path that includes an input and an output, a feedback path coupled to the output and the input, and a sensor that is between the input and the output and generates a sensor signal. The error signal generator is for generating an error signal and for providing the error signal to the control circuit. The forward path is configured to generate an output signal based on the sensor signal and the error signal. The output signal is sent along the feedback path to the input of the forward path. The detector is for obtaining an intermediate signal from the forward path between the input and the output and for generating a control signal based on the intermediate signal. The forward path includes a control device to limit the output signal to a predetermined value. The detector is for controlling the control device using the control signal.

Hyatt neither discloses nor suggests the features of independent claim 1. To the contrary, Hyatt describes an analog memory system that includes different types of memories interfaced with interfaced controllers that typically provide accessing, writing, and addressing capabilities. As Hyatt explains:

> Alternately, interface controllers having first address and last address registers or first address and block length registers for accessing blocks of information from computer peripherals such as a disk memory are well known in the art, wherein these memory block access arrangements can be implemented for the analog ROM of the present invention from the teachings herein. (Hyatt, col. 28, lines 31-38.)
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> Interface controllers can be used for bubble memory 801 and CCD memory 802 similar to interface controllers used for well-known prior art rotating memories. (Id., col. 47, lines 49-51.)
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> Because rotating memories are conventionally interfaced to processors with interface controllers, the interface controller typically provides accessing, writing, and addressing capabilities. (Id., col. 48, lines 18-21.)

Accordingly, Hyatt's interface controller registers addresses and allows accessing of different memories in its analog memory system. Nowhere does Hyatt disclose a controller that includes a control circuit, an error signal generator, and a detector, each having the features of claim 1.

The Examiner refers to circuit 996 in FIG. 9 of Hyatt as a control circuit. Applicant points out that Hyatt's circuit 996 in FIG. 9 is a refresh circuit that refreshes memory output signals. As Hyatt explains:

> Refresh circuit 996 refreshes memory output signal 936 for output and for recirculation as signal 960. The output signal from the memory system may be the unrefreshed memory signal 936 or the refreshed signal 960, shown as outputs from memory 932 by arrows pointing out of the memory system to other systems. Refreshed signal 960 may be recirculated back to the input of memory 932 under control of selection circuitry and a FET electronic switch 947. (Id., col. 58, line 63 – col. 59, line 4.)

Thus, Hyatt's refresh circuit 996 is not a control circuit. Further, as explained above, Hyatt's controller provides accessing, writing and addressing capabilities to memories. Refresh circuit 996 performs a function, i.e., refreshing memory outputs, which is different than the controller. Therefore, Hyatt's refresh circuit 996 and interface controllers are independent components of its analog memory system, both structurally and functionally.

The Examiner further refers to input signals 504 and 505 and output signals 506 and 507 as the input and output of the control circuit (circuit 996) that is included in Hyatt's controller. As explained above, circuit 996 is not a control circuit, nor is it part of a controller. Further, input signals 504 and 505 and output signals 506 and 507 do not belong to circuit 996. Instead, these inputs and outputs are part of register 501, as Hyatt explains:

> The circuits shown in FIG. 12B will now be discussed for the embodiment of the reverberation unit of FIG. 5, wherein input signal 504 (FIG. 5) may be the same as analog input signal AI 504 (FIG. 12B) and output signal 507 (FIG. 5) may be the same as analog output signal 507 (FIG. 12B) and wherein register 501 (FIG. 5) may include CCD memory 932, refresh circuit 996, and the other circuitary shown in FIG. 12B. (Id., col. 104, lines 59-66)
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> Delay is provided with CCD register 501 under control of a clock such as a three-phase clock described herein. (Id., col. 18, lines 18-20.)
>
> Register 501 may be any well-known register, but in a preferred embodiment is a CCD shift register and may have a plurality of parallel inputs 504 and 505 and/or a plurality of parallel outputs 506 and 507. (Id., col. 18, lines 45-48.)

Therefore, register 501 is not a control circuit and is different from circuit 996. The inputs and outputs of register 501 are not parts of circuits 996.

The Examiner also refers to a transducer as a sensor between the input and the output. Without conceding that refresh circuit 996 is a control circuit and a transducer is a sensor, Applicant further points out that nowhere does Hyatt disclose a transducer between the input and output of refresh circuit 996. The portion of Hyatt cited by the Examiner reads:

> The term signal is herein intended to include electrical signals, charge signals, current signals, acoustic signals, illumination signals, magnetostrictive signals, sonic signals, magnetic signals, and other known signals which may be sensed such as with a transducer and which may be processed such as with a filter. (Id., col. 116, lines 56-61.)

Thus, Hyatt describes that signals can be sensed by a transducer. However, Hyatt does not disclose that the transducer is between the input and output of refresh circuit 996, nor does its disclose that the transducer is a sensor to generate a sensor signal, as recited by claim 1.

The Examiner also cited the following text of Hyatt as evidence of Hyatt's disclosure of an error signal generator that generates an error signal and that provides the error signal to the control circuit, wherein the forward path generates an output signal based on the sensor signal and the error signal, the output signal being sent along the feedback path to the input of the forward path:

> For simplicity of discussion, an OTA servo arrangement is provided for scale factor compensation. This arrangement is merely exemplary of other servo arrangements and other scale factor arrangements which can be implemented by those skilled in the art from the teachings herein. Servo 1113 comprises OTA 1116 for amplifying the sampled signal from sample-and-hold circuit 961A. The sampled signal is compared with reference signal V.sub.REF using differential amplifier 1117 for generating a feedback error signal to OTA gain controlling input I.sub.ABC. Servo 1113 is connected so that a deviation of the amplified sampled signal from the V.sub.REF signal is indicative of an amplitude error condition. The output signal from differential amplifier 1117 is a servo error signal which is fedback to control the gain of OTA 1116 with the amplifier bias current (ABC) I.sub.ABC to adjust the output signal from OTA 1116 to the amplitude of reference signal V.sub.REF. Gain controlling current I.sub.ABC is also used to compensate the memory output signal 936 by controlling gain or OTA 1114 with signal 1115 to OTA gain control input I.sub.ABC to compensate for scale factor errors in memory output signal 936, generating compensated output signal 960. The I.sub.ABC current signal to OTAs 1114 and 1116 can be generated by well known current generators such as with well known current sources; shown functionally as differential amplifier 1117. (Id., col., line 59 – col. 93, line 17.)

The system that includes feedback error generation described in the above text is part of to a memory compensation arrangement, as Hyatt explains:

> For simplicity of discussion, scale factor compensation and bias compensation will be discussed in various combinations and configurations relative to FIG. 11 to exemplify the more general features of the present invention. Memory signal compensation arrangement 1100 is shown in FIG. 11 having various alternate compensation configurations. (Id., col. 91, lines 62-68.)
>
> FIGS. 11A to 11C illustrate different configurations 1100 of scale factor and bias compensation in block diagram form. (Id., col. 92, lines 1-3.)

Therefore, the system that includes feedback error generation as cited by the Examiner is not part of Hyatt's controller. Further, Hyatt's feedback error signal is not sent along the feedback path to the input of the forward path, as recited by claim 1. To the contrary, Hyatt's feedback error signal is generated to OTA 1116 to gain controlling input I_{ABC} and sent along the forward path to the output signal 936 to compensate the memory signal 936.

The Examiner next refers to detectors 643 and 645 of Hyatt as anticipating the detector that obtains an intermediate signal from forward path between the input and output and generates control signal based on the intermediate signal, as recited by independent claim 1. Without conceding that Hyatt's detectors 643 and 645 are part of a control, nowhere does Hyatt disclose that detectors 643 and 645 obtain an intermediate signal from forward path between the input and output and generates control signal based on the intermediate signal. In fact, Hyatt's detectors 643 and 645 relates to a computer subroutine or a threshold detector. As Hyatt explains:

> A computer subroutine will now be discussed with reference to FIG. 6D to illustrate how computer 112R (FIGS. 6A and 6C) may be programmed to control multiple-block memory accesses and to provide different control parameters for different blocks. (Id., col. 28, lines 41-45.)
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> Digital detector circuits 643 and 645 have been discussed as digital detectors with reference to FIG. 6D. Alternately, detectors 643 and 645 may be implemented as analog detectors such as Schmidt triggers or other analog threshold detectors for an analog output signal sample embodiment. Control circuitry including compositor control 632, one-shot 651, counters 616-619, decoder 622, and decoder 628 which have been discussed above for a digital embodiment but may also be used in conjunction with the analog or hybrid CCD memory embodiment. (Id., col. 82, lines 34-44.)
>
> Schmidt trigger threshold detector may be used as a one-bit ADC 934 to detect whether the output information 936 is above or below a threshold, indicative of a binary one or a binary zero condition. If above the threshold, Schmidt trigger ADC 934 may restore the amplitude to an upper amplitude magnitude and, if below a threshold, Schmidt trigger ADC 934 may restore the signal to a lower amplitude magnitude. (Id., col. 76, lines 43-51.)

Accordingly, instead of an intermediate signal, detectors 643 and 645 obtains an output signal and adjusts the signal according to a threshold.

Finally, the Examiner cited the following text as anticipating the features of independent claim 1 that includes the forward path comprises a control device that limits the output signal to a predetermined value, the detector controlling the control device using the control signal:

> The instant feature is implemented by multiplexing a discharge signal into the CCD memory and shifting this signal through the memory to provide the discharge function. This predetermined discharge signal may be part of a memory record preamble to discharge the memory prior to recirculation similar to the preamble described relative to FIG. 9 for refresh reference signals. (col. 99, lines 36-43.)
>
> Digital detector circuits 643 and 645 have been discussed as digital detectors with reference to FIG. 6D. Alternately, detectors 643 and 645 may be implemented as analog detectors such as Schmidt triggers or other analog threshold detectors for an analog output signal sample embodiment. Control circuitry including compositor control 632, one-shot 651, counters 616-619, decoder 622, and decoder 628 which have been discussed above for a digital embodiment but may also be used in conjunction with the analog or hybrid CCD memory embodiment. (Id., col. 82, lines 34-44.)

However, Hyatt's predetermined discharge signal is part of a memory record preamble to discharge the memory prior to recirculation. The predetermined discharge signal does not belong to a control device included in a forward path of a control circuit. Nor is it a value that limits the output of a control circuit.

As such, independent claim 1 is believed to be allowable over Hyatt. Independent claims 8 and 16 include subject matter similar to independent claim 1 and are also believed to be allowable over Hyatt.

The dependent claims 2-7, 9-15, are 17-20 are allowable at least for the reasons discussed with respect to independent claims 1 and 10. Although it is believed that the dependent claims

define patentably distinct features, given the distinctiveness of the respective independent claims, the dependent claims are not discussed here in detail.

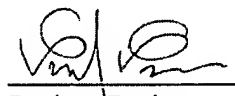
It is believed that all of the pending claims have been addressed. However, the absence of a reply to a specific rejection, issue or comment does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above may not be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

In view of the foregoing remarks, the entire application is now believed to be in condition for allowance, and such action is respectfully requested at the Examiner's earliest convenience.

Please apply any deficiency in fees or credit any overpayment to deposit account 06-1050, referencing Attorney Docket No. 14603-013US1.

Respectfully submitted,

Date: March 21, 2008



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